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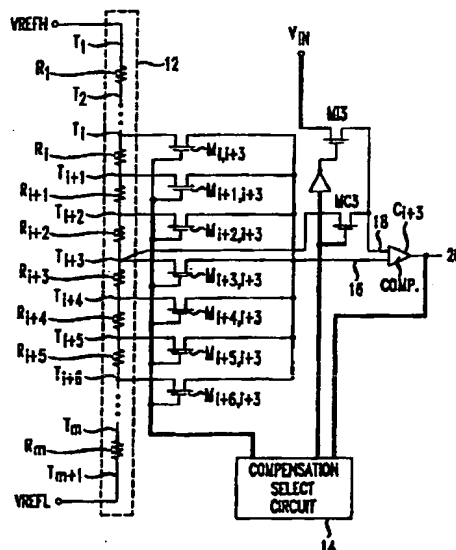
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(54) Comparator-offset compensating AD-converter

(57) An integrated circuit for converting an analog signal to a digital signal includes a resistor string (12) comprised of a plurality of serially coupled resistors (R) coupled between a high voltage reference (VREFH) and a low voltage reference (VREFL). Intermediate taps (T) are defined at the junctions of the resistors in the resistor string. At least one comparator (C_{i+j}) has first and second inputs (16,18) and an output (20). The first input (16) of the comparator is capable of being selectively coupled to preselected ones of the intermediate taps. The second input (18) is capable of being switched between an unknown analog input (V_{IN}) in conversion mode and a predetermined tap (T_{i+3}) that provides a nominal voltage at the second input in calibration mode. A selection circuit (14) for sequencing through the preselected ones of the intermediate taps selects one of the preselected ones of the intermediate taps as selected tap for compensating for the offset of the at least one comparator. The selection circuit stores the selected tap for subsequent use during operation of the circuit.

FIG. 2



Description

Technical Field

This invention relates generally to analog-to-digital converters (ADC), and more particularly to such converters that compensate for comparator offset.

Background of the Invention

ADC converters employing many comparators generating a thermometer code which can be decoded to binary output for high speed analog-to-digital conversion are referred to as flash converters. One input of each comparator of this type converter is connected to a unique reference voltage to which the input signal is to be compared. The number of unique reference voltages is usually equal to the number of comparators used. These unique reference voltages may be provided by a series resistor string coupled between a high reference voltage, and a low reference voltage that may be grounded. Unless a gain stage is provided, the difference between the high reference voltage and the low reference voltage should be equal in the maximum level that the input voltage to be converted can assume.

As integrated circuits move towards lower power, supply voltages decrease. As supply voltage decreases, the maximum voltage that can be converted also decreases as does the difference between the high reference voltage and the low reference voltage and the reference voltage developed across individual resistors representing a least significant bit (LSB) falls to within the offset voltage of comparators generating the thermometer code. When the offset voltage of a comparator is greater than one LSB a discontinuity occurs in the thermometer code developed at the collective outputs of the comparators. For the thermometer code to be meaningful, something must be done to overcome the comparator offset and restore thermometer code continuity.

One known technique provides for trim to match components in a comparator to reduce or eliminate comparator offset. Trimming occurs once at the time of production and, is thereafter fixed to the conditions that existed at the time of trim. Alternate techniques trade off speed of operation of the converter for area of silicon required to manufacture the converter. For one such technique, the array of comparators in a converter alternate between conversion operation and being offset nulled. This technique reduces the speed of conversion by the amount of time required for offset nulling. A variation on this technique provides a duplicate array of comparators in a converter such that the two arrays of comparators alternate in operation. While one array is being used for conversion the other array is being offset nulled. This variation requires a larger silicon area to accommodate the duplicate array of comparators and more power to operate the duplicate array of comparators.

What is desired is a technique to overcome comparator offset to provide a meaningful thermometer code without making a tradeoff with respect to speed, area of silicon, or power consumption.

Summary of the Invention

In accordance with the present invention, an integrated circuit for converting an analog signal to a digital signal includes a resistor string comprised of a plurality of serially coupled resistors coupled between a high voltage reference and a low voltage reference. Intermediate taps are defined at the junctions of the resistors in the resistor string. At least one comparator has first and second inputs and an output. The first input of the comparator is capable of being selectively coupled to preselected ones of the intermediate taps. The second input is capable of being switched between an unknown analog input in conversion mode and a predetermined tap that provides a nominal voltage at the second input in calibration mode. A selection circuit for sequencing through the preselected ones of the intermediate taps selects one of the preselected ones of the intermediate taps as a selected tap for compensating for the offset of the at least one comparator. The selection circuit stores the selected tap for subsequent use during conversion operation of the circuit.

Brief Description of the Drawing

Figure 1 is a schematic diagram of an analog-to-digital converter including comparator offset compensation in accordance with the present invention; Figure 2 is a schematic diagram of a portion of the schematic diagram of Figure 1 showing the resistor string and a single comparator; Figure 3 is a schematic diagram of an analog-to-digital converter similar to Figure 1, with the resistor string tapped at locations other than incremental least significant bit locations; and Figure 4 is a schematic diagram showing two pairs of switches to reverse the inputs of a comparator.

Detailed Description

Figure 1 shows a schematic diagram of an analog-to-digital converter 10 including comparator offset compensation in accordance with the present invention. The ADC includes a resistor string coupled between a high voltage reference, and a low voltage reference that is typically ground. Banks of switches, shown as MOS transistors, couple taps surrounding a nominal tap to a common input of a respective comparator. The other comparator input is switchable between the nominal tap when in calibration, and an unknown input voltage during conversion operation. The comparator outputs collectively provide a thermometer code that can be converted to any binary form to provide a digital output.

Resistor string 12 is comprised of a user determined number of resistors in series. The number of resistors, m , is typically $2^n - 1$, where n is the number of bits of the converter. The resistors are thusly noted R_1 through R_m . The resistors may be of identical resistance. With a voltage applied across resistor string 12, a voltage gradient is developed across the resistor string and the same voltage drop, equal to one LSB, develops across each resistor in the string. The resistance values of the resistors comprising resistor string 12 are application dependent and can be readily selected by one skilled in the art based on a variety of parameters such as the power to be dissipated, the potential across the resistor string, and the number of resistors in the resistor string. The resistor string is coupled between a high voltage reference, V_{REFH} , and a low voltage reference, V_{REFL} , that may be grounded. Each resistor junction as well as each resistor-voltage source junction defines a tap T_1 through T_{m+1} . Switches, shown in the illustrative embodiment as MOS transistors, each couple a tap with an input of a respective comparator, C_1 through C_m .

Operation of the offset compensation is best understood with reference to Figure 2 in which a portion of the schematic diagram of Figure 1 is illustrated. The normal voltage, assuming no comparator offset voltage, to cause the output of a comparator C_{i+3} to change state (i.e., the switching threshold) is the voltage at T_{i+3} of resistor string 12. In the presence of offset in comparator C_{i+3} , the actual voltage to cause the output of comparator C_{i+3} to change state may be higher or lower than the nominal voltage. Since the offset of any comparator C_1 through C_m is not known in advance, but in the range of offset is known through experience in a given technology, allowance is made for the actual voltage that causes the comparator output to change state to be higher or lower than nominal voltage, within the range of offset. For example, a six bit flash converter having one volt across resistor string 12 is comprised of 63 identical resistors. Each resistor has a 15.6 millivolt drop across it representing one LSB. A flash converter typically has as many comparators as resistors. Typical offset range for a comparator is ± 50 millivolts thus, without some form of compensation, a thermometer code developed at the output of the comparators is meaningless. Since the offset voltage can range in the illustrative embodiment to approximately plus or minus three times (generally h times) the voltage of an LSB, having the capability to shift the input voltage to a comparator along the resistor string, up or down the equivalent of three LSB's, would compensate for the offset voltage of a comparator.

In accordance with the present invention, each comparator has first and second inputs 16 and 18, and an output 20 at which an output signal is presented. Input signals applied to inputs 16 and 18 are compared and the output indicates which is larger. While various conventions may be used, the illustrative embodiment will describe the output signal of a comparator as high

when the input signal on input 18 is greater than the input signal on input 16.

Calibration of comparator C_{i+3} is typical of the calibration of all comparators in converter 10. To calibrate comparator C_{i+3} , a voltage is impressed across resistor string 12. Compensation select circuit 14 turns transistor M13 off to isolate input 18 of comparator C_{i+3} from the unknown analog input voltage to be converted, V_{IN} , and turns transistor MC3 on to couple input 18 of comparator C_{i+3} to the nominal voltage at tap T_{i+3} .

Compensation select circuit 14 is capable of switching various voltages along the resistor string to be the second input signal at second input 16. The number of voltages capable of being switched will vary, but typically will include voltages both greater than and less than the nominal voltage at tap T_{i+3} . In the illustrative embodiment, h voltages above nominal voltage, nominal voltage, and h voltages below nominal voltage, for a total of $(2h+1)$ voltages or seven voltages can be independently switched to second input 16.

Switches $M_{i,i+3}$ through $M_{i+6,i+3}$ are systematically switched, one at a time, to couple associated tap voltages, T_i through T_{i+6} , on resistor string 12 to be the input signal to second input 16. The tap voltages shown in the illustrative embodiment of Figures 1 and 2 are incremental LSB values, but the invention is not so limited. See for example Figure 3. When sequencing through switches $M_{i,i+3}$ through $M_{i+6,i+3}$ from bottom to top (as shown in Figure 2), the first switch associated with a tap voltage which causes comparator C_{i+3} to change state from a one to a zero is considered to provide an input voltage that compensates for the offset of comparator C_{i+3} . Similarly, when sequencing through switches $M_{i,i+3}$ through $M_{i+6,i+3}$ from top to bottom, the first switch associated with a tap voltage which causes comparator C_{i+3} to change state from a zero to a one is considered to provide an input voltage that compensates for the offset of comparator C_{i+3} . Other sequencing methods are possible. The switch that provides an input voltage that compensates for the offset of comparator C_{i+3} remains closed and all other switches $M_{i,i+3}$ through $M_{i+6,i+3}$ remain open for the calibration. The address of the switch that couples a voltage that compensates for the offset of comparator C_{i+3} is stored in memory, such as in compensation select circuit 14. The memory may be any type of memory including registers and flash memory.

Having completed compensation of comparator C_{i+3} , compensation select circuit 14 sequences to the next comparator and repeats the above process, storing in memory the address of the switch that couples an input voltage that compensates for the offset of the next comparator. This sequencing continues until compensation select circuit 14 has identified and stored the address of a switch to couple a voltage to each comparator that compensates for the offset voltage of that comparator.

One of ordinary skill in the art can develop logic to sequence through the comparators and the switches

associated with each comparator to identify the switch that couples a voltage to compensate for the offset of each comparator, and to store the address of each such switch in a memory or register.

The offset calibration can be continued to both ends of resistor string 12. For the first h comparators at the top of the resistor string 12, this technique more readily compensates for comparator offset that is positive and for the last h comparators associated with resistors at the bottom of resistor string 12, this technique more readily compensates for comparator offset that is negative. To provide for the full $2h+1$ voltages such that each comparator is compensated to within one LSB, it may be necessary to reverse the inputs to one or more of the top three and bottom three comparators. As is known in the art, the inputs to a comparator can be reversed using two pairs of switches as illustrated in Figure 4. The pairs of switches, controlled by compensation select circuit 14, need only be supplied for the h comparators associated with resistors at the top of resistor string 12 and the h comparators associated with resistors at the bottom of resistor string 12. This technique could extend to all comparators.

Alternatively, the offset calibration can be extended to all comparators by extending the resistor string by h resistors at both ends and introducing a gain error that can be compensated for using known techniques.

The output of each comparator is provided to compensation select circuit 14 and thermometer-to-binary converter 20. The collective outputs of the comparators are converted to any known binary form by thermometer to binary converter 20 for serial or parallel digital output as shown in Figures 1 and 3.

An alternative embodiment ADC 10' shown in Figure 3 provides a distributed resistor string 12'. Adjacent taps are separated by less than one LSB. The preselected taps coupled through switches to a comparator are separated by one LSB.

While the illustrative embodiment of the invention has been described as coupling a single tap to the first input of a comparator, more than one tap may be coupled to the first input at the same time, resulting in an effective tap, in accordance with U.S. Patent Application Serial No. 08/327174 filed October 21, 1994, the disclosure of which is hereby incorporated by reference. Coupling more than one tap to the first input would occur such as when, the voltage drop across a resistor in the resistor string is greater than one LSB. The number of taps and which taps are coupled simultaneously to the first input of a comparator would depend on the incremental voltage drop required to obtain an LSB.

In an alternative embodiment, instead of using resistor string 12 to generate the nominal calibration voltages, an accurate voltage can be impressed on V_{IN} , with V_{IN} coupled to input 18 of comparator C_{i+3} by transistor M13. Since the calibration voltage is provided by V_{IN} , in the alternate embodiment transistor MC3 need not be present. The remainder of the circuit in Figures 1 and 2 would remain and operate as described above. It

is recognized that as many accurate voltages would be required as there are comparators, and the voltages would have to be at least as accurate as the number of bits it is desired to convert and the alternative embodiment could not as conveniently be recalibrated. Furthermore, the alternative embodiment compensates for both comparator offset and resistor string non-linearities.

The illustrative embodiment of the invention is particularly useful in integrate circuits that utilize this technique. Such integrated circuits have the advantages of high speed low power operation in a small area of silicon to provide offset compensation for comparators. Calibration as described above can occur at wafer test, can be user initiated, or can be initiated upon power-up of the converter. Factors that suggest the need for recalibration short term include changes in ambient temperature, and long term include degradation of an integrated circuit. As compensated, the switching thresholds of the comparators need not be more accurate than one LSB. At wafer test, on any chip that a switch can not be identified for each comparator to provide compensation, that chip can be discarded. Variations in the switch settings stored by compensation select circuit 14 of chips at wafer test is an inference that there is a change in the manufacturing process. When an integrated circuit is calibrated in the manner described above and at least one comparator is identified for which a switch can not be identified to provide offset compensation, an error flag may be set.

Claims

1. An integrated circuit for converting an analog signal to a digital signal, including a resistor string (e.g., 12) coupled between a high voltage reference (V_{REFH}) and a low voltage reference (V_{REFL}), the resistor string (e.g., 12) comprising a plurality of serially coupled resistors (R_1 through R_m) intermediate taps (T_1 through T_{m+1}) defined at the junctions of the resistors (R_1 through R_m) in the resistor string (e.g. 12), and at least one comparator (C), the at least one comparator (C) having first (e.g., 16) and second inputs (e.g., 18) and an output (e.g., 20), characterized in that
 - the first input (e.g., 16) of the comparator (C) capable of being selectively coupled to preselected ones of the intermediate taps (T_1 through T_{m+1}), the second input (e.g., 18) capable of being switched between an unknown analog input in operation mode and a predetermined tap that provides a nominal voltage at the second input (e.g., 18) in calibration mode; and
 - a selection circuit (e.g., 14) for sequencing through the preselected one of the intermediate taps (T_1 through T_{m+1}) to select at least one of the preselected ones of the intermediate taps (T_1 through T_{m+1}) as a selected tap for compensating for the offset of said at least one comparator (C),

- the selection circuit (e.g., 14) for storing the selected tap for subsequent use in the conversion mode.
2. An integrated circuit for converting an analog signal to a digital signal, including a resistor string (e.g., 12) coupled between a high voltage reference (V_{REFH}) and a low voltage reference (V_{REFL}), the resistor string (e.g., 12) comprising a plurality of serially coupled resistors, intermediate taps (T_1 through T_{m+1}) defined at the junctions of the resistors (R_1 through R_m) in the resistor string (e.g., 12), and a plurality of comparators (C), each of the comparators (C) having first and second inputs (e.g., 16 and 18) and an output, characterized in that
 - the first input (e.g., 16) of each of said plurality of comparators (C) capable of being selectively coupled to one of several preselected taps associated with each comparator (C), the second input (e.g., 18) of each of said plurality of comparators (C) capable of being switched between an unknown analog input in conversion mode and a predetermined tap that provides a nominal voltage at the second input (e.g., 18) in calibration mode; and
 - a selection circuit (e.g., 14) for sequencing through the preselected taps to select at least one of the several preselected taps as a selected tap for compensating for the offset of each of said plurality of comparators (C), the selection circuit (e.g., 14) for storing the selected tap for each of the plurality of comparators (C) for use in of the conversion mode.
 3. An integrated circuit for converting an analog signal to a digital signal, including a resistor string (e.g., 12) coupled between a high voltage reference (V_{REFH}) and a low voltage reference (V_{REFL}), the resistor string (e.g., 12) comprising a plurality of serially coupled resistors, intermediate taps (T_1 through T_{m+1}) defined at the junctions of the resistors (R_1 through R_m) in the resistor string (e.g., 12), and at least one comparator (C), the at least one comparator (C) having first and second inputs (e.g., 16 and 18) and an output, characterized in that
 - the first input (e.g., 16) of the at least one comparator (C) capable of being selectively coupled to several preselected taps, the second input (e.g., 18) of the at least one comparator (C) capable of being switched between a reference voltage in calibration mode and an unknown analog input voltage (V_{IN}) in conversion mode;
 - a selection circuit (e.g., 14) for sequencing through the preselected taps to select at least one of the preselected taps as a selected tap for compensating for the offset of said at least one comparator (C), the selection circuit (e.g., 14) for storing the selected tap for use in the conversion mode.
 4. An integrated circuit for converting an analog signal to a digital signal, including a resistor string (e.g., 12) coupled between a high voltage reference (V_{REFH}) and a low voltage reference (V_{REFL}), the resistor string (e.g., 12) comprising a plurality of serially coupled resistors, intermediate taps (T_1 through T_{m+1}) defined at the junctions of the resistors (R_1 through R_m) in the resistor string (e.g., 12), and a plurality of comparators (C), each of the comparators (C) having first and second inputs (e.g., 16 and 18) and an output, characterized in that
 - the first input (e.g., 16) of each of said plurality of comparators (C) capable of being selectively coupled to one of several preselected taps associated with each of the comparators (C), the second input (e.g., 18) of each of the comparators (C) capable of being switched between a reference voltage in calibration mode and an unknown analog input voltage (V_{IN}) in conversion mode; and
 - a selection circuit (e.g., 14) for sequencing through the preselected taps to select at least one of the several preselected taps as a selected tap for compensating for the offset of each of the comparators (C), the selection circuit (e.g., 14) for storing the selected tap for each of the plurality of comparators (C) for use in the conversion mode.
 5. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the preselected ones of the intermediate taps (T_1 through T_{m+1}) the first input (e.g., 16) is capable of being selectively coupled to is an odd number.
 6. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the preselected ones of the intermediate taps (T_1 through T_{m+1}) the first input is capable of being selectively coupled to includes said predetermined tap that provides a nominal voltage at the second input (e.g., 18).
 7. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the preselected ones of the intermediate taps (T_1 through T_{m+1}) the first input (e.g., 16) is capable of being selectively coupled to includes at least one tap in the resistor string (e.g., 12) above said predetermined tap that provides a nominal voltage at the second input (e.g., 18).
 8. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the preselected ones of the intermediate taps (T_1 through T_{m+1}) the first input (e.g., 16) is capable of being selectively coupled to includes at least one tap in the resistor string (e.g., 12) below said predetermined tap that provides a nominal voltage at the second input (e.g., 18).

9. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the preselected ones of the intermediate taps (T_1 through T_{m+1}) the first input (e.g., 16) is capable of being selectively coupled to includes at least one tap in the resistor string (e.g., 12) above said predetermined tap, and at least one tap in the resistor string (e.g., 12) below said predetermined tap that provides a nominal voltage at the second input (e.g., 18).
10. An integrated circuit as recited in any of claims 1, 2, 3 or 4, further characterized by
a thermometer code scale circuit (e.g., 22)
for receiving the output of said at least one comparator (C), the thermometer code scale circuit (e.g., 22) for converting the output of said at least one comparator (C) to a binary output.
11. An integrated circuit as recited in any of claims 1, 2, 3 or 4, characterized in that the first input of the comparator (C) is capable of being selectively coupled to preselected ones of the intermediate taps (T_1 through T_{m+1}), one at a time.

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FIG. 1

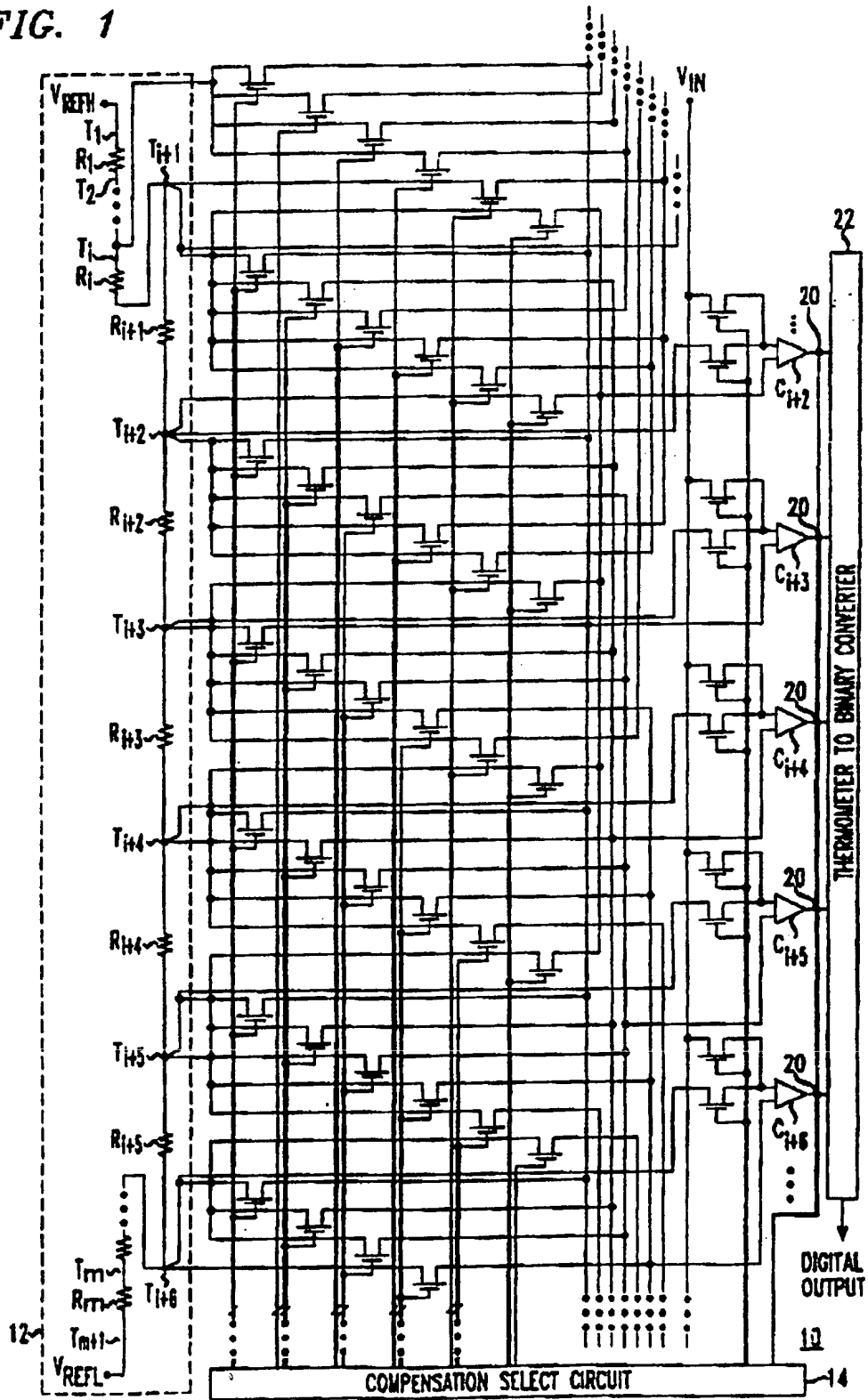


FIG. 3

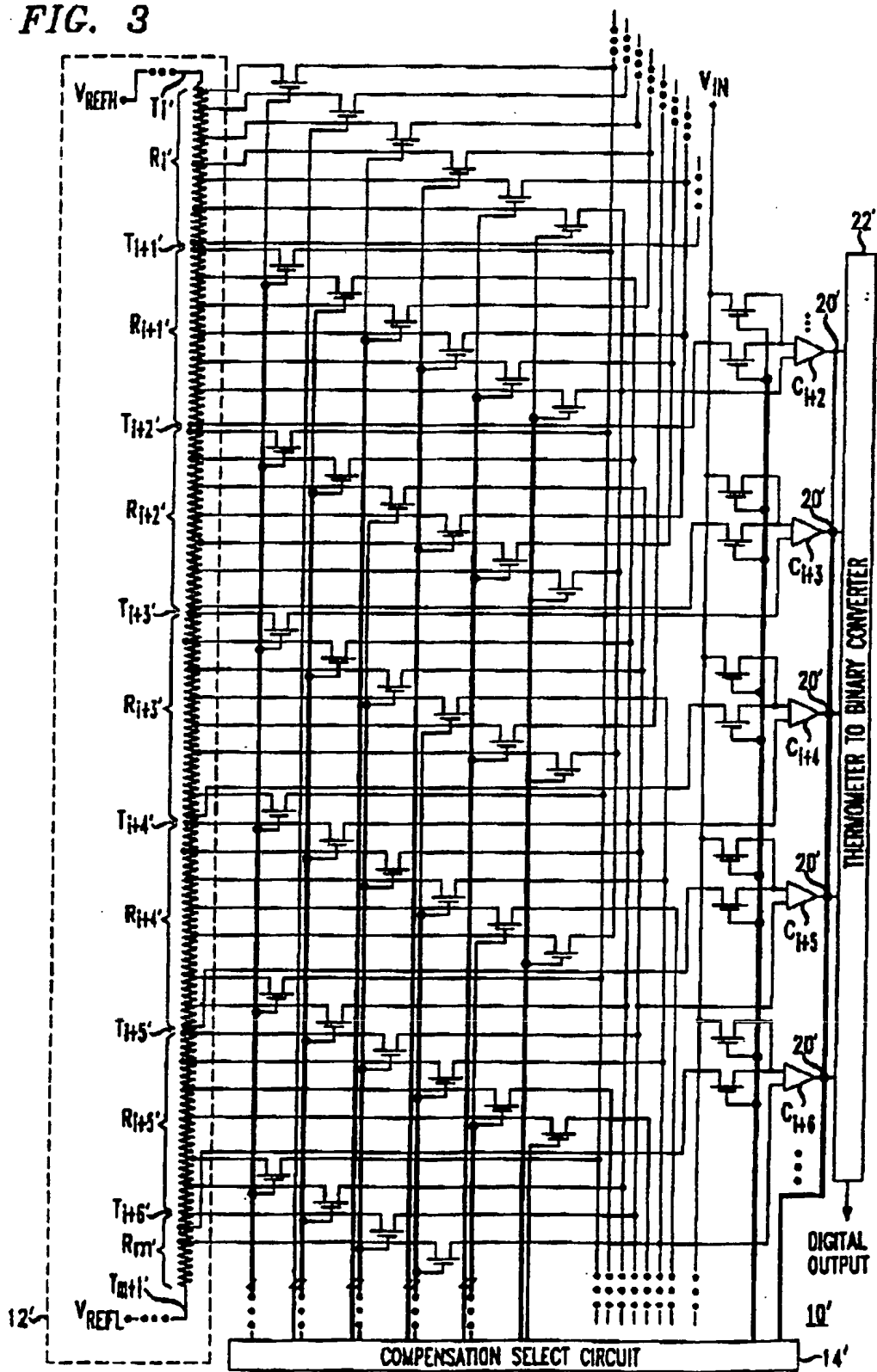
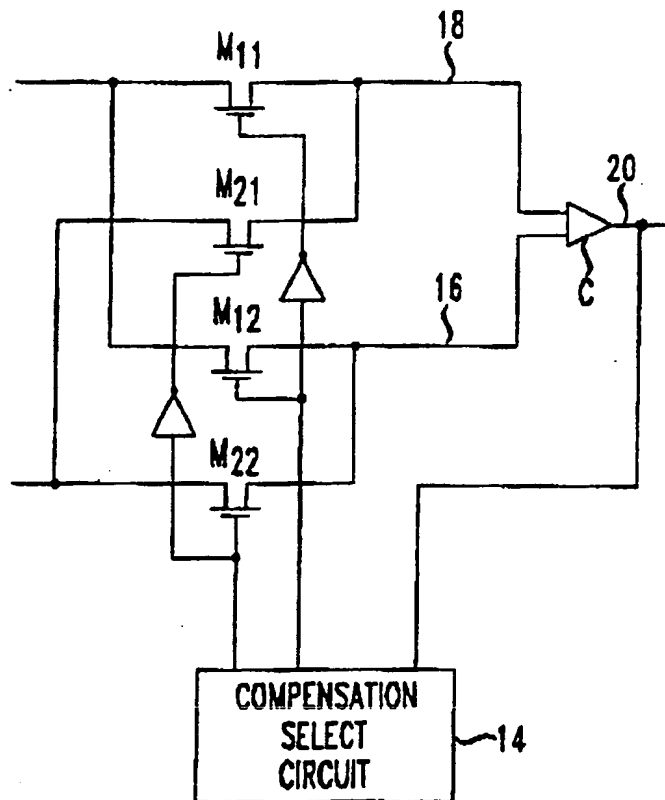


FIG. 4





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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 1243

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 012 no. 026 (E-577) ,26 January 1988 & JP-A-86 023798 (HITACHI) 11 August 1987, * abstract *	1	H03M1/06 H03M1/36
A	---	3,4	
A	US-A-4 794 374 (KOIKE) * the whole document *	1,2	
A	---		
A	EP-A-0 054 079 (DEUTSCHE ITT INDUSTRIES) * the whole document *	1,2	
A	---		
A	EP-A-0 101 571 (TOKYO SHIBAURA DENKI KABUSHIKI) -----		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03M
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22 May 1996	Examiner Guivol, Y
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

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